REV	ZONE	ECO #	REVISION	APPD	DATE
A		R119	INITIAL RELEASE		
B	Sh2 Sh9 Sh10 Sh11	R467	Chgd Vcc standby volt from 3.0 volts, Icc standby from 10ua. Chgd OSC FUNCT from 30pf and 10pf. Added 6.1 Chgd 7.2 and Note 3 from Vcc=4.0v.	QH. KLB VW	2/86 2/86 2/86

ENGINEERING SPECIFICATION

P/N: 343-0042-B

DESCRIPTION: IC, RAM, 256 Byte Serial Clock

MARKINGS: Part is to be marked with part number 343-0042 and current revision level, copyright designator and date code.

EXAMPLE: 343-0042-B
© APPLE 84,85
xxxx

The Device Specification (Description and Electrical Test Spec) shall be filed in Corporate Document Control and cannot be removed without proper authorization.

NOTE: Manufacturer's name or logo is also to be marked on part. The order of the markings is not important.

DRAWING NUMBER 343-0042-B SH1 OF 11

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. DECIMALS .X ± ___ .XX ± ___ .XXX ± ___ ANGLES XX.X ± ___ FRACTIONS ± ___ DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.	DRAWN BY J. Trieves DATE 11/13/84 CHECKED BY D. Hon DATE 11/84 APPROVED BY J. Trieves for J. Weber DATE 11/29/84 RELEASED BY DATE 11/29/84	apple computer inc.	
MATERIAL: ___		TITLE IC, RAM, 256 BYTE SERIAL CLOCK	
FINISH: ___		SIZE A	DRAWING NUMBER 343-0042-B
NEXT ASSY.		SCALE: ___	SHEET 1 OF 12

1.0 FEATURES

- Real Time Clock; a 32 bit seconds counter
- 32.768 kHz crystal oscillator for the real time clock
- 256 bytes of RAM for standby scratchpad storage
- serial I/O for minimum pin count (8 pin standard mini-dip package)
- independent data clock input (shift strobe) for serial port
- Vcc operating range of 4.0 to 5.25 volts
- Vcc standby voltage of 2.0 volts.
- Icc standby < 15μa
- No minimum frequency for data clock input
- plug-in replacement for serial clock and RAM chip (343-0040)

2.0 GENERAL DESCRIPTION

This device contains a 256 byte RAM plus a real time clock addressed as 4 additional bytes. The device will continue to keep track of time, and retain data, down to a standby voltage of 2.0 volts. The device communicates with a microprocessor via a simple bidirectional serial port. The commands are to read or write the byte registers containing the RAM and clock. A 32.768 kHz crystal provides a frequency base for the real time clock. Only 3 lines are required for serial processor communication. These are CE* (chip enable), I/O (input-output), and SCK (I/O data valid clock). SCK rejects noise at the switching point for 8ns minimum.

3.0 PIN DESCRIPTION

Pin	Name	Function
1	CKO	1 Hz square wave open drain output
2	XTAL1	crystal oscillator inverter input
3	XTAL2	crystal oscillator inverter output
4	Vss	ground
5	CE*	chip enable input (low level active)
6	I/O	bidirectional input and open drain data output
7	SCK	serial data clock input
8	Vcc	+ supply voltage

4.0 PACKAGE DESCRIPTION

The package is a standard 8 pin dual-in-line package, with 0.1 inch pin spacing, and 0.3 inch pin row spacing.

5.0 TECHNICAL DESCRIPTION

5.1 OVERVIEW

The device is selected by CE* which is kept low throughout the operation. Commands and data are sent serially through the I/O pin. Input to the device must meet specified set-up and hold times relative to the rising edge of SCK. Data output from the device changes after the falling edge of SCK. There are four possible operations: standard read, standard write, extended read, and extended write. All operations begin with the input of a command byte to the device. This determines whether the operation is a read or write and whether it is standard or extended. If it is an extended read or write, an extended memory address byte is input to the device. Then for all operations a byte is input to the device for writes or output from the device for reads. Figures 2, 3, and 4 show waveforms for the possible operations.

5.2 CHIP ENABLE FUNCTION

When CE* is brought high the device is not selected and the I/O pin is in the high impedance condition. When CE* is brought low the device expects to recieve a command byte. This command byte may be followed by the input of an extended memory address byte. Then a data byte is written into or read out of a register within the device. If CE* is brought high before the complete command and data transfer into the device has taken place, the operation will be aborted and no data will be written to the register. (Clock register counting is independent of CE*)

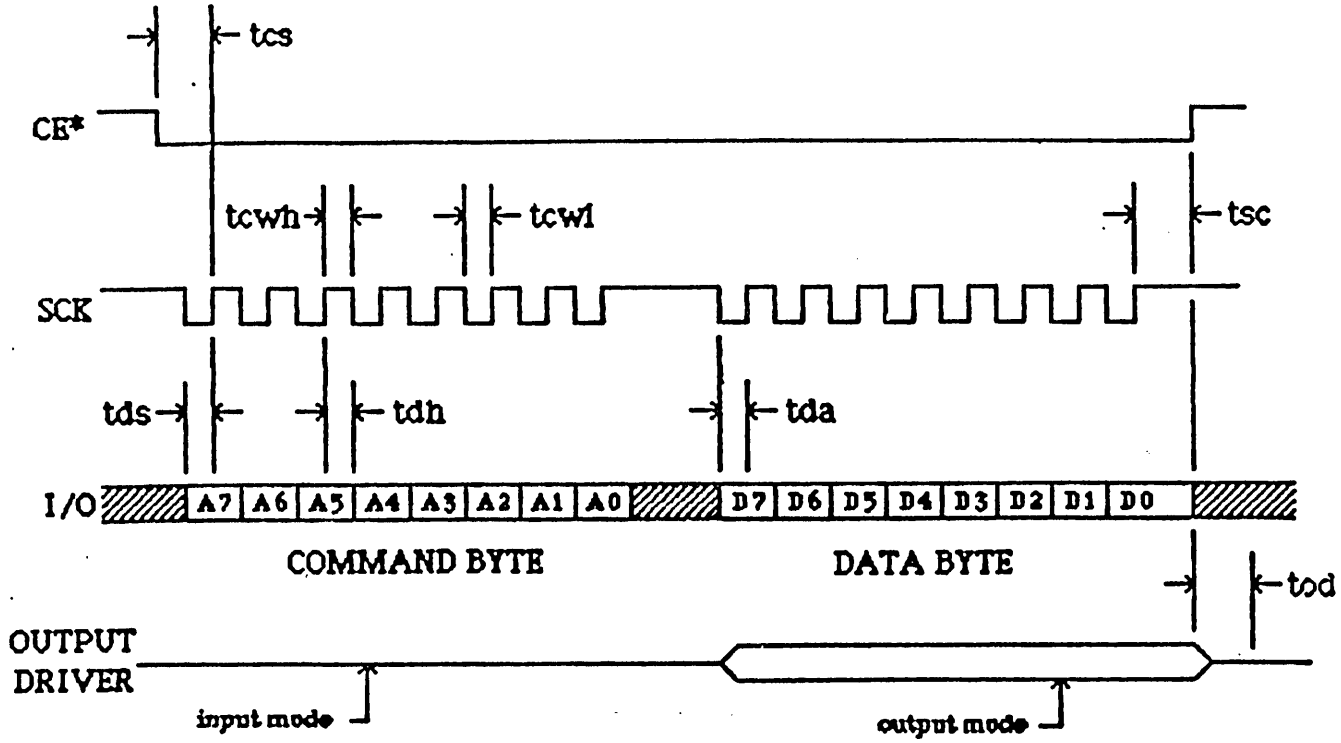
5.3 COMMAND BYTE

The command byte defines the data direction (read or write) and selects the register to be accessed or defines the extended memory sector number. The encoding of the command byte is shown in Figure 1. Addresses that are not listed are not used. The data will be unspecified if unlisted addresses are read and no registers will be disturbed if unlisted addresses are written. Do not use unlisted addresses as they may be used in future versions. Commands are identical to those used in SERIAL CLOCK AND RAM CHIP (343-0040) except (1) the extended memory designator command has been added and can be used on this device only, (2) the code for write-protect bit address (bit1, bit0) was 01 in the 343-0040 clock but now are don't care. Address the write-protect bit only with the code 00110101 to be software compatible with 343-0040.

Code Bit								Function or Register
7	6	5	4	3	2	1	0	
R/W*	0	0	x	0	0	0	1	Seconds reg. address (least significant byte)
R/W*	0	0	x	0	1	0	1	Seconds reg. address
R/W*	0	0	x	1	0	0	1	Seconds reg. address
R/W*	0	0	x	1	1	0	1	Seconds reg. address (most significant byte)
0	0	1	1	0	0	0	1	Test bit address
0	0	1	1	0	1	X	X	Write-protect bit address
R/W*	0	1	0	a	a	0	1	4 RAM addresses
R/W*	1	a	a	a	a	0	1	16 RAM addresses
R/W*	0	1	1	1	a	a	a	Extended memory designator and sector number

Figure 1. Command Byte Codes (x indicates don't care)

STANDARD READ



STANDARD WRITE

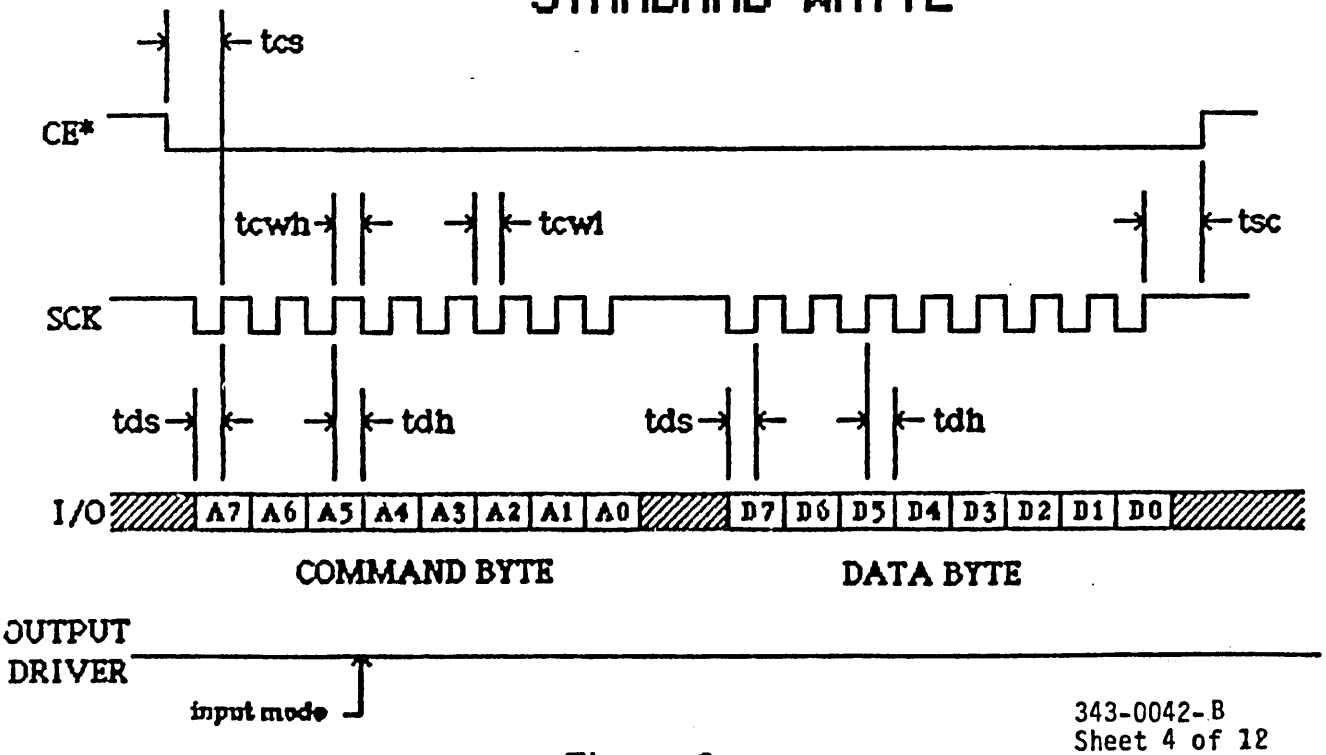


Figure 2

EXTENDED READ

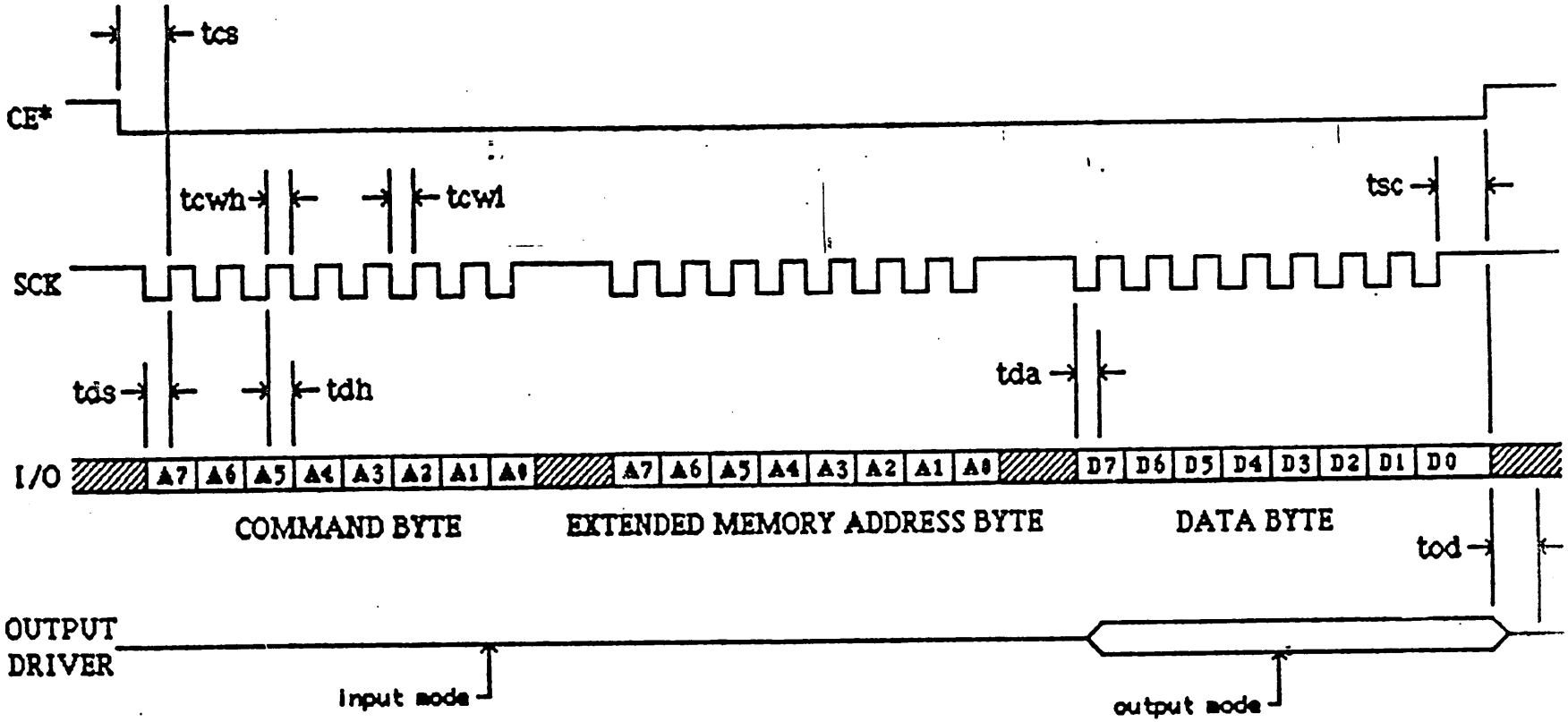


Figure 3

343-0042-B
Sheet 5 of 12

EXTENDED WRITE

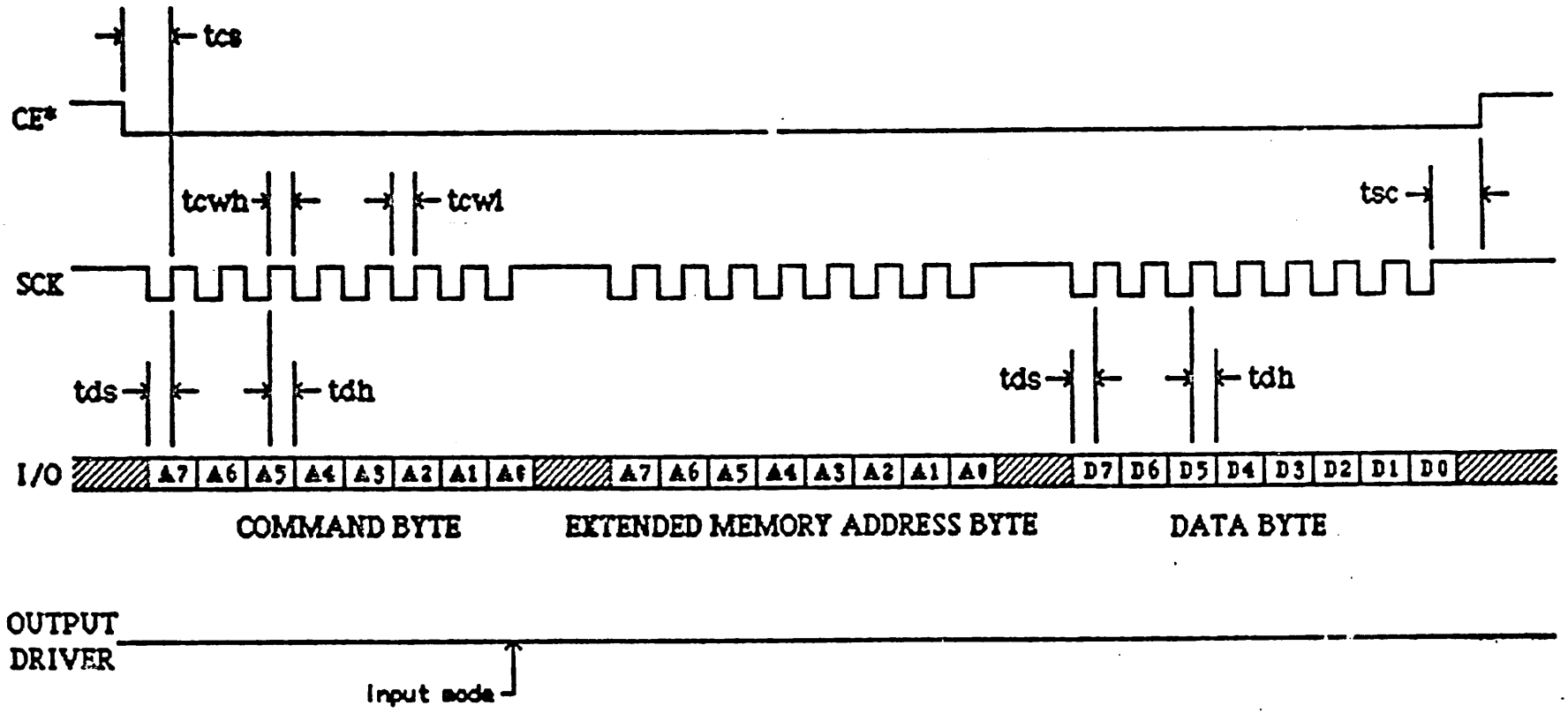


Figure 4

5.4 EXTENDED MEMORY ADDRESS BYTE

If the command byte designates an extended memory operation, the next byte will be input and contain 5 bits of X-address. The RAM is structured as 8 sectors (Y-decode) of 32 bytes (X-decode).

Code Bit								Function or Register
7	6	5	4	3	2	1	0	
x	a	a	a	a	a	x	x	RAM X-Address

Extended Memory Address Code (x indicates don't care)
Figure 5.

Twenty bytes can be addressed directly or via extended memory addressing. They map into the RAM in sector 0 using the same X-Address decoder as the extended memory operation where code bits 2-6 of the command byte are used instead of code bits 2-6 of the exended memory address byte.

5.5 DATA TRANSFER

The next byte of data following the command byte (or extended memory address byte) will be either input to or output from the addresed register. In the input mode the register will be updated when a complete byte has been received. The internal format of the registers is shown in Figure 6

Register Format								Register Name
7	6	5	4	3	2	1	0	
MSB	———	seconds	———				LSB	Seconds byte
tst	*	*	*	*	*	*	*	Test bit
wp	*	*	*	*	*	*	*	Write-protect bit
			N.A.					RAM byte

Clock and Control Register Format
(Bits marked * do not physically exist)
Figure 6.

5.6 REGISTERS

5.6.1 SECONDS REGISTERS

The clock consists of a 32 bit counter that increments once per second following the rising edge of CKO. The clock is accessable as four registers of 8 bits each. Writing one clock register may cause the next most significant register to increment spuriously, so the clock should be written least significant byte to most significant byte. There is a small probability that the time will be set incorrectly if a register counts from 255 to 0 while the next most significant byte is being written. Therefore the clock should be read for verification. In addition, the clock may increment during a read operation resulting in the incorrect time. Reads should be done until two successive times (all 4 bytes) are identical.

5.6.2 RAM REGISTERS

The RAM is structured as 8 blocks (sectors) each having 32 rows and 8 columns. The sector number (Y-decode) connects the proper block to the internal data bus for data transfers to the 8 columns. The sector number is contained in the extended memory command otherwise it is 0. The code bits 2-6 of the command byte or the extended memory address byte are used to decode the row (X-decoder).

5.6.3 WRITE PROTECT REGISTER

The write-protect register is only 1 bit wide. When true it prevents writing into any register except the write-protect bit register. The write-protect bit will be set by writing a 1101010x (D5 or D4) data pattern and will be reset by writing a 0101010x (55 or 54) data pattern. The 8th data bit is a don't care because the actual write to the register takes place when SCK is low just before the 8th data bit is clocked in. (Note that in the 20-byte clock chip the data patterns were D5 to set write-protect and 55 to clear write-protect with the actual write occuring as the 8th data bit is clocked in.) Use only D5 to set and 55 to reset the write-protect bit in order to be software compatible with 343-0040.

5.6.4 TEST BIT REGISTER

The test bit register is only 1 bit wide. It is used for production testing only and must always be set to zero for the clock counters to function as specified. A zero should be written to this register during device initialization. The write-protect bit must be cleared before the test register can be written. The test bit is set by writing a data pattern with bit7 = 1 and reset by writing a data pattern with bit7 = 0. The other bits are don't care. When the test bit is set, the one-second counter is reset and the seconds counter increments after the rising edge of XTAL1 instead of CKO.

5.7 [illegible] - OUTPUT

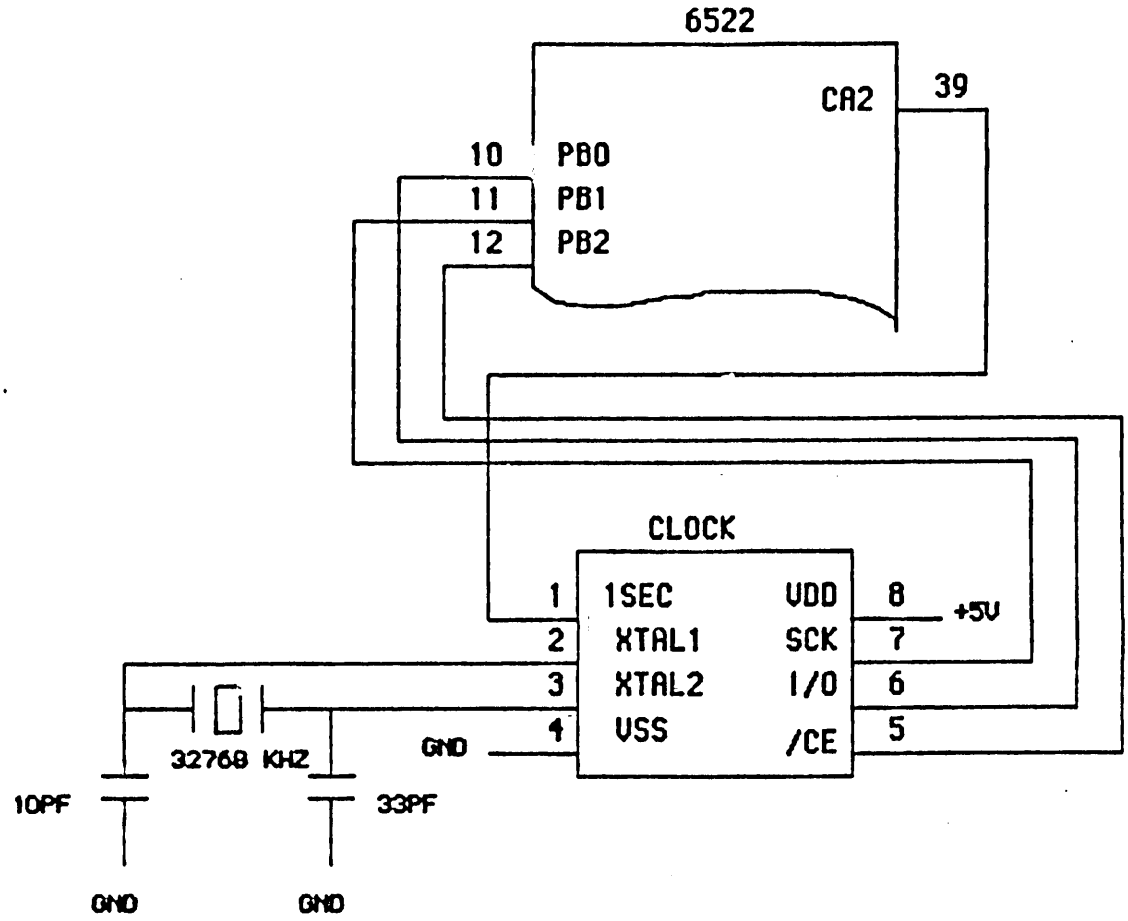
Data is transferred serially in 8 bit (1 byte) groups with the most significant bit (bit7) first, and the least significant bit (bit0) last, for both input and output. In the input mode, the I/O pin is held in a high impedance condition, and data on the I/O pin is sampled on the rising edge of SCK. In the output mode the I/O pin is driven by the device, with data changing on the falling edge of SCK. The first 8 bits transferred to the device after the falling edge of CE* define the command byte. They may be followed by an extended memory address byte. The next 8 bits are the data byte.

The device is in the input mode during the command byte and the optional extended memory address byte, and then will either change to output mode or stay in the input mode depending on the command byte. The I/O pin remains in the high impedance condition until after the falling edge of SCK which follows the eighth rising edge of SCK which clocks in the last bit of the command byte or until after the falling edge of SCK which follows the 16th rising edge of SCK which clocks in the last bit of the extended memory address byte. Any additional SCK cycles following the data byte (first 16 or 24 with extended memory) will be ignored in input mode and generate unspecified data in output mode.

6.0 OSCILLATOR FUNCTION

The oscillator requires only a crystal and 2 external capacitors to oscillate. Pins 2 and 3 connect to an external 32.768 kHz tuning fork crystal and 2 tank capacitors. The active component of the oscillator is an inverter whose input is pin 2 and output is pin 3. The inverter is biased into its active region by an internal feedback resistor. The feedback resistor will be in the range of 5-15 megohm measured with Vcc = 4.0v at 25°C. The inverter's gain, output impedance, and phase shift shall be such that the inverter will oscillate with a Daiwa Crystal Corporation DT-38 crystal or equivalent with 10pf to ground at pin 2 and 30pf to ground at pin 3 with Vcc=4.0 volts minimum.

6.1 APPLICATION NOTE



CLOCK CONNECTIONS IN MAC

NOTE: 1SEC AND I/O PINS NEED EXTERNAL PULL-UPS OR PULL-UPS LOCATED AS PART OF THE INPUT PINS OF THE 6522.

7-31-85

7.0 ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Voltage on any pin relative to Vss..... -0.5 to +8v
Operating temperature, ambient..... 0 to +75°C
Storage temperature..... -35 to +125°C

7.2 DC Electrical Characteristics

Sym	Parameter	Min	Typ	Max	Units	Notes
Vcc	supply voltage	4.0	5.0	5.25	V	1
Vcs	standby voltage	2.0	-	-	V	1
Icc	supply current	-	-	500	µA	2
Ics	standby current	-	-	15	µA	3
Iil	input leakage	-	-	±10	µA	4
Vih	logic 1 input	2.0	-	-	V	9
Vil	logic 0 input	-	-	0.8	V	9
Ioh	output high leakage	-	-	10	µA	5
Vol	logic 0 output	-	-	0.4	V	6,7,9
OSC0	XTAL2 sink current	14.0	-	50.0	µA	10
OSC1	XTAL2 source current	14.0	-	50.0	µA	11
Ilat	latch-up current	-	-	±25	mA	8
Vosc	supply voltage for oscillator start-up	4.0	-	5.25	V	

Notes:

1. All voltages referenced to Vss.
2. At Vcc=5.25v, XTAL1=32.768 kHz, CE*, and I/O all within 0.5v of Vss or Vcc, SCK toggling at 800 kHz with a rise (fall) time < 100ns.
3. At Vcc=3.5v XTAL1=32.768 kHz, CE*, SCK, and I/O all within 0.2 volts of Vss.
4. At Vcc=5.25v, inputs=0 to 5.25v.
5. At Vcc=5.25v, I/O in output mode, CKO and I/O=5.25v.
6. Vol measured at 1.6 mA sink current.
7. CKO and I/O are open drain outputs which require external pullups.
8. Inputs and outputs must not exceed the range Vss-0.5v to Vcc+0.5v. Outside this range they must source or sink at least Ilat without causing SCR latch-up.
9. At Vcc from 4.0v to 5.25v
10. Temperature=25°C, Vcc=4.0v, XTAL2=2.0v, XTAL1=4.0v.
11. Temperature=25°c, Vcc=4.0v, XTAL2=2.0v, XTAL1=0.0v.

7.3 AC Electrical Characteristics

Sym	Parameter	Min	Typ	Max	Units	Notes
cp	pin capacitance	-	-	12	pf	
fx	crystal frequency	28	32.768	37	kHz	
tcs	CE*, FE to SCK, RE	1.0	-	-	µs	
tds	I/O valid to SCK, RE	0.5	-	-	µs	setup
tdh	SCK, RE to I/O invalid	0.5	-	-	µs	hold
tda	SCK, FE to I/O valid	-	-	0.5	µs	access
tsc	SCK, RE to CE*, RE	1.0	-	-	µs	
tod	CE*, RE to I/O open	-	-	1.0	µs	
tcwl	SCK low	0.5	-	-	µs	
tcwh	SCK high	0.5	-	-	µs	
tceh	CE* high	1.0	-	-	µs	reset
trej	SCK noise reject window	8.0	-	160	ns	

FE = falling edge (high to low transition)
RE = rising edge (low to high transition)

Refer to Figures 2, 3, and 4.

7.4 Static Protection

This device will incorporate static protection on all inputs and outputs. The protection will be designed to provide protection against discharges of greater than 1 kV delivered by an equivalent-body discharge network of 100pf through 560 ohms.